IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAE-SUNG KIM, *et al.*

Serial No.:	10/767,281	Examiner:	WARREN, MATTHEW E.
Filed:	30 January 2004	Art Unit:	2815

For: NOVEL CONDUCTIVE ELEMENTS FOR THIN FILM TRANSISTORS USED IN A FLAT PANEL DISPLAY

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites, describes, and provides copies of the following art references. Under 37 C.F.R. §1.98(a)(2) however, copies of U.S. patent reference(s) are not provided.

US PATENT REFERENCE:

- United States Patent No. 5,747,879 to Rastogi, *et al.*, entitled *INTERFACE BETWEEN TITANIUM AND ALUMINUM-ALLOY IN METAL STACK FOR INTEGRATED CIRCUIT*, issued on 5 May 1998.
- United States Patent No. 6,083,830 to Yamadai, entitled *PROCESS FOR MANUFACTURING A SEMICONDUCTOR DEVICE*, issued on 4 July 2000.
- United States Patent No. 5,538,921 to Obeng, entitled *INTEGRATED CIRCUIT FABRICATION*, issued on 23 July 1996.
- United State Patent No. 6,414,738 to Fujikawa, entitled *DISPLAY*, issued on 2 July 2002. (previously filed in Information Disclosure Statement filed on 4 October 2005).

- United States Patent No. 6,255,706 to Watanabe, *et al.*, entitled *THIN FILM TRANSISTOR AND METHOD OF MANUFACTURING SAME*, issued on 3 July 2001. (previously filed in Information Disclosure Statement filed on 4 October 2005).
- United States Publication No. 2001/0002050 to Kobayashi, *et al.*, entitled *THIN-FILM TRANSISTOR ARRAY AND METHOD OF FABRICATING THE SAME*, issued on 31 May 2001.
- United States Publication No. 2001/0043174 to Yasukawa, entitled *LIQUID CRYSTAL PANEL SUBSTRATE, LIQUID CRYSTAL PANEL, AND ELECTRONIC EQUIPMENT AND PROJECTION TYPE DISPLAY DEVICE BOTH USING THE SAME*, issued on 22 November 2001.
- United States Publication No. 2002/0164860 to Yang, *et al.*, entitled *METHOD OF FABRICATING THIN-FILM TRANSISTOR*, issued on 7 November 2002.
- United States Publication No. 2002/0076574 to Cabral, Jr., *et al.*, entitled *INTERCONNECTS WITH TI-CONTAINING LINERS*, issued on 20 June 2002.

FOREIGN PATENT REFERENCE:

- European Patent Publication No. 1 001 463 to Cichy, *et al.*, entitled *ALUMINUM INTERCONNECTS FOR INTEGRATED CIRCUITS COMPRISING TITANIUM UNDER AND OVERLAYERS*, published on 17 May 2000 (with English abstract).

OTHER DOCUMENTS:

- European Office action for European Patent Application No. 04250862.2, issued on 26 January 2006.
- An article "Relationship between copper concentration and stress during electromigration in an Al(0.25 at. % Cu) conductor line" written by Kao, *et al.* published in American Institute of Physics, pp2516-2527 on 1 March 2003 (with English abstract).
- An article "VLSI Metallization using aluminum and its alloys" written by Pramanik,

et al., published in Physics & Technologies, pp 268-275 (with English abstract).

DISCUSSION

Rastogi US'879, according to the European Office action in applicant's European patent application Serial No. 04250862.2, discloses that an improvement in a metal stack used for interconnecting structures in an integrated circuit. The improvement comprises the entrapping in a titanium layer of nitrogen at the interface where the titanium layer contacts a bulk conductor layer such as an aluminum-copper alloy layer. The entrapped nitrogen prevents the formation of any substantial amount of titanium aluminide thereby reducing current densities and also improving the electromigration properties of the stack. As currently preferred, the nitrogen is entrapped in approximately the first 30Å of the titanium layer.

Yamadai US'830, discloses that a process for producing a semiconductor device comprising the steps of forming a titanium film having a orientation, forming a titanium nitride film on the titanium film to such a thickness as allows the titanium nitride film to follow the orientation of the titanium film, and forming an aluminum alloy film on the titanium nitride film, thereby to form a layer structure for wiring including the aluminum alloy film having a orientation.

Obeng US'921, discloses that after multilayer conductive stacks are defined in a semiconductor processing sequence, rinsing with a dilute solution of surfactants is performed to remove halogen residues which may ultimately contribute to subsequent undesirable corrosion of the stack.

Fujikawa US'738, discloses that in a display device such as a liquid crystal display device, in order to connect electrodes and wiring with a low resistance, the first titanium nitride film having a hexagonal crystal structure for preventing silicon diffusion is intervened between the drain region composed of a polycrystalline silicon film and the drain electrode composed of an aluminum film.

The second titanium nitride film having a hexagonal crystal structure which can be deposited by sputtering with the same target as that for the titanium film and the first titanium film is intervened between the transparent display electrode composed of an ITO film and the drain electrode composed of an aluminum film in order to ring them into ohmic contact. Since the second titanium nitride film is resistant to an etchant for the silicon oxide film and to an etchant for the ITO film, the drain electrode is protected when etching is performed.

Watanabe US'706, discloses that a thin film transistor wherein at least one of a gate electrode and/or a scanning line therefore and source/drain electrode and/or signal lines therefor comprises a laminated wiring structure in which a main wiring layer formed of a metal selected from Al and Cu or an alloy based on the metal is sandwiched between an underlying wiring layer and an overlaying wiring layer, the underlying and overlaying wiring layers being formed of a material based on a metal or alloy of metals and containing nitrogen, the metal being selected from Ti, Mo, W, Cr, Al and Cu, and the materials used in the underlying and overlaying wiring layers being different from each other. Alternatively, the underlying and overlaying wiring layers are formed of a material based on the same metal or alloy of metals and containing nitrogen, the metal being selected from Ti, Mo, W, Cr, Al and Cu, and contents of nitrogen in the underlying and overlaying wiring layers being different from each other. A method of manufacturing such a thin film transistor is also disclosed.

Kobayashi US'050, discloses that a thin-film transistor array includes a substrate, an electrically conductive portion, and a metal layer. The electrically conductive portion is made of one of indium tin oxide, indium oxide, and tin oxide. The electrically conductive portion and the metal layer are formed on a common surface of the substrate. The metal layer includes a first layer and a second layer. The first layer is made of one of aluminum and an aluminum alloy. The second layer extends on the first layer and is made of metal having an oxidization potential nobler than a

reduction potential of said one of indium tin oxide, indium oxide, and tin oxide in alkaline aqueous solution.

Yasukawa US'175,discloses that the present invention is a liquid crystal panel substrate that comprises; pixel units each having a pixel electrode, to be used as a reflective electrode and arranged in a matrix pattern on a substrate, and a switching element controlling a voltage applied to the pixel electrode; wherein between the pixel electrode and a conductive layer forming a terminal electrode of the switching element, a contact hole is provided for connecting the pixel electrode and the terminal electrode. A light-shielding layer, having an opening surrounding the portion in which the contact hole is formed, and having no opening in regions between a plurality of adjacent pixel electrodes, is formed between the pixel electrode and the conductiv4e layer. Harmful effects due to light leaking through a space between the pixel electrodes can thereby be prevented.

Yang US'860, discloses that a method of fabricating a thin-film transistor on an insulation substrate. A first conductive layer, a gate dielectric layer, a silicon layer and a doped silicon layer are formed on the insulation substrate. These four layers are patterned to form a gate and a gate line. A second conductive layer is formed over the insulation substrate. The second conductive layer and the doped silicon layer are patterned to form a source/drain region, a source/drain conductive layer and a source/drain line on both sides of the gate line. A protection layer is formed over the insulation layer, followed by a patterning step to form openings on the source/drain conductive layer and the source/drain line. A transparent conductive layer is formed on the protection layer and in the openings. After being patterned, a pixel electrode is formed, and a portion of the transparent conductive layer remains to electrically connect the source/drain line and the source/drain conductive layer. The method of fabricating the thin-film transistor can be applied to fabrication of fax machine, CIS such as scanner and various electronic devices. It can also be applied to fabrication of normal thin-film transistor flat panel display such as liquid crystal display (LDC) and organic light emitting diode (OLED).

Cabral US'574, discloses that an electrical conductor for use in an electronic structure si disclosed which includes a conductor body that is formed of an alloy including between about 0.001 atomic % and about 2 atomic % of an element selected from the group consisting of Ti, r, In, Sn and Hf; and a liner abutting the conductor body which is formed of an alloy that includes Ta, W, Ti, Nb and V. The invention further discloses a liner for use in a semiconductor interconnect that is formed of a material selected from the group consisting of Ti, Hf, In, Sn, Zr and alloys therof, $TiCu_3$, $Ta_{1-x}Ti_X$, $Ta_{1-X}Hf_X$, $Ta_{1-X}In_{XY}$, $Ta_{1-X}SN_X$, $Ta_{1-X}Zr_X$.

Cochy EP'463, discloses that an interconnect for an integrated circuit includes an underlayer comprising titanium having reduced contamination for improved electromigration and for supporting another layer. An intermediate layer comprising aluminum is deposited over the underlayer. An overlayer comprising titanium having increased contamination relative to the underlayer to provide a reduced sheet resistance is applied over the intermediate layer. The resulting interconnect has improved reliability and functionality. A method is also provided.

Kao discloses that Synchrotron-based x-ray microbeam fluorescence and diffraction have been sued for *in situ* measurements of Cu concentration and biaxial stress in a 200-μm-long, 10-μm-wide Al(0.25 at. % Cu) conductor line with 1.5-μm-thick SiO_2 passivation during electromigration. Measurements over 48 h with T = 300 °C and $J = 1.5 \times 10^5$ A/cm show that a stress gradient of 3 MPa/μm develops over the upstream 130 μm of line length where Cu concentration drops below 0.15 at. %, and a 10-μm-long void develops at the cathode end of the line, but little change in stress occurs over the downstream 70 μm of line length where Cu concentration remains above 0.15 at %. These experimental results have been reproduced by a finite element model in which the downstream Cu transport is accompanied by a counter flow of Al in the upstream direction, and downstream Al motion is blocked where the local Cu concentration is above ~0.15 at %. Defect mediated coupling between Al and Cu diffusive flows, e.g., Cu-vacancy binding, is proposed as the cause for the counterflow of Al when the Cu concentration is above the critical concentration, and as the mechanism by which Cu reduces the rate of electromigraion damage in Al(Cu) conductor lines.

Pramanik discloses that aluminum and its alloys are and will continue to be used in IC metallization for making contacts to silicon, as well as for interconnections. The first part of "VLSI Metallization Using Aluminum and Its Alloys" ran in the January issue of *Solid State Technology*. It examined the key material concepts that determine the effectiveness and reliability of Al to silicon/polysilicon contacts and Al/Al-alloy interconnects in VLSIC. These include: (1) solubility of Al in Si; (2) diffusion of Si in Al; (3) effectiveness of Al as a transport medium for Si; (4) reactivity of Al; (5) electromigraion; (6), resistivity. Various aspects of pure Al metallization were analyzed suing these concepts. The problem of Al spiking through Si, as well as the influence of substrate orientation, cleanliness of contracts, and stresses in the Si on Al spiking were discussed. In addition, Part I examined the contact resistance of Al to p- and n-type substrates, along with the dependence of Al-Si contact resistance on surface dopant concentrations. The influence of Al-Si interactions on the properties of Al Schototkys was also discussed. In the second part of the article, which follows, other aspects of Al metallization, Al-Si metallization, and alternate Al contact schemes are discussed. This discussion should aid the reader in understanding the limitations of Al metalization, as well as ways of improving Al matallization in future process applications.

Pursuant to 37 CFR §1.97(d), the undersigned attorney hereby certifies that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign patent application not more than three (3) months prior to the filing of the statement.

The citation of the foregoing references is not intended to constitute an assertion that other or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-ranging and thorough search of the relevant art.

No fee is incurred by this Statement.

Respectfully submitted,

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U.S. PATENT DOCUMENTS

EXAMINER	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,747,879	05/98	*Rastogi, et al.*			
	6,083,830	07/00	*Yamadai*			
	5,538,921	07/96	*Obeng*			
	6,414,738	07/02	*Fujikawa*			
	6,255,706	07/01	*Watanabe et al.*			
	2001/0002050	05/01	*Kobayashi, et al.*			
	2001/0043175	11/01	*Yasukawa*			
	2002/0164860	11/02	*Yang et al.*			
	2002/0076574	06/02	*Cabral, Jr., et al.*			

FOREIGN PATENT DOCUMENTS						TRANSLATION	
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	YES	NO
	EP 1 001 463	05/00	EUROPE			Abstract	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	European Office Action of the European Patent Application No. 04250862.2, mailed on 26 January 2006
	An article "Relationship between copper concentration and stress during electromigration in an Al(0.25 at. % Cu) conductor line" written by Kao, *et al.* published in American Institute of Physics, pp2516-2527 on 1 March 2003 (with English abstract).
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EXAMINER:	*DATE CONSIDERED:*

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.